SIMULATION OF 2.4 GHZ LOW-POWER CMOS LC QUADRATURE VOLTAGE CONTROLLED OSCILLATOR

Ms.SREEJA B.S and Ms.RADHA S

1Research Scholar, Sathyabama University, 2Prof and Head Department of ECE, SSN College of Engineering
sreejaabs@gmail.com, radhas@ssn.edu.in

ABSTRACT

This paper presents the simulation analysis of a 2.4 GHz Quadrature Voltage Controlled Oscillator (QVCO), for low-power, low-voltage applications. Cross coupled LC VCO (Inductor-Capacitor Voltage Controlled Oscillator) topology is utilized to realize QVCO. With the passive coupling achieved from the MOS transistors, power consumption is minimized while maintaining a small chip area. The variable capacitors and the inductors are designed using ANSYS and imported through DAC components in ADS (Advanced Design software). Accurate simulation of the QVCO is performed in the software environments and the results are provided. This QVCO provides quadrature signals at 2.4 GHz, achieves a peak to peak voltage of 0.65 volts with a simulated low power consumption of 5.8 mA from a power supply voltage of 0.6 volts. The simulated QVCO produces frequency tuning from 2.1 GHz to 2.60 GHz (20.83%) with a control voltage varying from 0-0.3 volts. The output power level of the QVCO is -7 dBm, with an improved predicted quality factor of 60 and a phase noise of -134 dBc/Hz, 1MHz far from the carrier frequency.

KEY WORDS: Variable capacitor, output voltage swing, low power consumption, ultra low supply voltage, Quadrature Voltage Controlled Oscillator, passive coupling

1. INTRODUCTION

The fast growing market in wireless communications has led to the need for low-power, low-noise voltage controlled oscillators. Especially for mobile wireless communications, low power operations are of very importance as the battery lifetime depends on the power consumption. Quadrature signals can be generated by feeding the differential outputs of the VCO to a poly phase filter [1,2], letting the VCO work at double the desired frequency and pass through frequency division [3,4], and coupling identical LC VCO circuits [5,6] to each other. The poly phase filter approach introduces substantial power consumption due to the attenuation by the resistance and the capacitance in the circuit. The frequency dividing approach avoids the pushing/pulling effect on the VCO, however, the existence of frequency divider and high frequency VCO result in increased power consumption.

A more attractive approach to direct quadrature synthesis relies on the possibility of effective coupling of two identical LC VCO circuits. The first coupling approach is the best known parallel coupling [7], where coupling between the two VCOs is enforced by transistors. While this coupling
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delivers low power, low amplitude and phase errors, it produces high phase noise. Introducing a phase shifter as reported in [8] offers better phase noise performance, however it increases the power consumption. Several other coupling techniques have been reported like back gate coupling [9], super-harmonic coupling [10], and transformer coupling [11]. In addition to this current reused QVCOs are also proposed [12]. However these approaches have their own merits and demerits, the urge of low power design of QVCO while maintaining low phase and amplitude errors still exists.

In this work an attempt is made to make use of the VCO, reported [13,14], to design a low power QVCO.

2. PROPOSED QVCO TOPOLOGY

The QVCO is designed to oscillate at 2.4 GHz, and to determine the impact on the performance parameters. Fig. 3(a) shows the LC VCO employed in this work. LC VCO provides outstanding phase noise and jitter performance at high frequencies compared to other topologies. Cross coupled pair LC VCO topology is selected for this design due to its high output voltage swing, balanced differential output and symmetrical structure. From the well known theory of oscillators, the positive feedback transistors M3 and M4 are used to achieve negative input resistance, with which positive resistance of LC resonant circuit might be eliminated bringing on zero-dampen oscillating property. PMOS transistors M1 and M2 are used to generate the required bias current. However, this topology provides the above merits, it contains an inductor and a varactor in its tank circuit which are large area components. In order to reduce the die area of the resonant circuit, MWCNT based pulse inductor is integrated with Micro scale varactor.

In order to reduce the required supply voltage and to eliminate additional noise contribution, the tail current transistors in a conventional cross-coupled VCO can be replaced by on-chip inductors [15].

![Figure 1](image_url)

(a) Schematic of the coupling Structure of QVCO  
(b) Equivalent circuit model of the coupling structure

Figure 1 : Schematic of the coupling Structure of QVCO  (b) Equivalent circuit model of the coupling structure
In this work the tail current transistors are replaced with MWCNT bundle based inductor. For an enhanced voltage swing under an ultra-low supply voltage, the capacitive-feedback technique can be employed [16]. The capacitive feedback loop is established by $C_1$ and $C_2$. Due to the use of the on-chip inductor and the capacitive feedback loop, the drain and source voltages can swing above the supply voltage and below the ground potential. Consequently, the output swing of the VCO is enhanced, leading to a superior close-in phase noise. Since the feedback capacitors are employed in the source terminals of the cross-coupled transistors, a more effective controlled mechanism of the tank resonance is presented. Therefore, a reasonable frequency tuning range can be achieved even with a reduced voltage range for the controlled signal. The variable capacitors $C_A$, $C_B$, and $C_C$ represent the Micro scale varactor and $C_B$ is modelled as two series capacitances to maintain the symmetry of the circuit. $L_1$ and $L_2$ are modelled as on-chip inductors. Fig. 3(b) shows the circuit diagram of the quadrature LC VCO. Two identical LC VCO circuits together with the coupling structure as shown in Fig. 1, are utilized to generate quadrature phase sinusoidal signals. The transistors are biased at zero dc current and operate as passive elements. Note that the coupling transistor is replaced by parallel $RC$ network in Fig 2. The design parameters of the simulated VCO are listed in Table 1.
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Figure 3: (a) Schematic of the proposed LC CMOS VCO showing the replacement of tail current transistors and the feedback gate capacitance (b) QVCO structure

Table 1: Design Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Design Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS Transistors</td>
<td></td>
</tr>
<tr>
<td>$M_3$</td>
<td>10.5 µm/ 0.6um  N=50</td>
</tr>
<tr>
<td>$M_4$</td>
<td>10.5 µm/ 0.6um  N=50</td>
</tr>
<tr>
<td>$M_5$</td>
<td>6 µm/ 0.6um    N=30</td>
</tr>
<tr>
<td>$M_1$</td>
<td>6 µm/ 0.6um    N=30</td>
</tr>
<tr>
<td>Coupling Transistor</td>
<td></td>
</tr>
<tr>
<td>$L_P$</td>
<td>0.61 nH</td>
</tr>
<tr>
<td>Micro Scale varactor</td>
<td>9 pF</td>
</tr>
<tr>
<td>$C_1$</td>
<td>10 µF</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>2.8 mA</td>
</tr>
<tr>
<td>$R_P$</td>
<td>150 Ω</td>
</tr>
<tr>
<td>$g_m$</td>
<td>$\geq 6.67$ mS + (safety factor 1.5)</td>
</tr>
</tbody>
</table>
Using laplace transform analysis the approximated transfer function (single ended output to input) can be derived as,

\[
\frac{V_o(s)}{V_i(s)} = \frac{-g_m(b_3 s^2 + b_4 s + b_5)}{a_0 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_4}
\]  \hspace{1cm} (9)

where the coefficients of the numerator and denominator are as follows:

\[
\begin{align*}
C_e &= C_2 / 2C_B + R / C \\
b_0 &= L_1 L_2 R_1 R_2 C_e \\
b_1 &= L_1 L_2 R_1 \\
b_2 &= L_4 R_1 R_2 \\
\end{align*}
\]

\[
\begin{align*}
a_0 &= L_1 L_2 R_1 R_2 C_A C_e \\
a_1 &= L_1 L_2 C_1 (R_1 C_A + R_2 C_A + R_2 C_e) \\
a_2 &= R_3 R_2 C_1 (L_2 C_A + L_2 C_A + L_2 C_e) \\
a_3 &= C_1 (L_3 R_3 + L_4 R_4 + g_m L_3 R_1 R_2) \\
a_4 &= C_1 R_1 R_2
\end{align*}
\]  \hspace{1cm} (10)

The circuit oscillates if equation (9) is equal to -1, and at the oscillation frequency \( \omega_o \),

\[
g_m \left( -b_2 \omega_o^4 + j b_4 \omega_o^4 + b_5 \right) = a_0 \omega_o^4 - j a_1 \omega_o^3 \\
\left( -a_2 \omega_o^2 + j a_3 \omega_o + a_4 \right)
\]  \hspace{1cm} (12)

With proper assumptions and simplifications the oscillation frequency can be approximated as

\[
\omega_o = \sqrt{\frac{1}{L_2 C_A} + \frac{2C_1(C_A + C_e)}{L_1 C_A C_B}}
\]  \hspace{1cm} (13)

\[
g_m = \frac{a_0 \omega_o^3 - C_1 (L_4 R_3 + R_3 L_2)}{R_1 R_2 (L_2 - L_1) + b_3 \omega_o^2}
\]  \hspace{1cm} (14)

Assuming \( L_1 = L_2 = L \) and \( R_1 = R_2 = R \), equation (13) and (14) can be simplified as,

\[
\omega_o = \sqrt{\frac{1}{Lp} \left[ \frac{1}{C_A} + \frac{2C_1(C_A + C_e)}{C_A C_e} \right]}
\]  \hspace{1cm} (15)

\[
g_m = \frac{1}{R_p} \left[ 1 + \frac{4(C_A / C_e) \omega_o^2}{C_1 + L_p(C_A / C_e)} \right]
\]
From equation (13) it is seen that the oscillation frequency has two parts, in its theoretical derivation. As conventional LC Voltage Controlled Oscillators, $\sqrt{\frac{1}{L_2 C_A}}$ contributes the major part of the oscillation frequency and the second part $\sqrt{\frac{2C_1(C_A + C_e)}{C_A C_e}}$ further enhances the oscillation frequency. However, the fixed capacitance $C_f$ degrades the oscillation frequency compared to [18], $\omega_0$ could be still improved by the numerator part $2(C_A + C_e)$. From equation (15) it is noticed that the fixed capacitance $C_f$ increases (since $< 1$) the trans-conductance which helps us to initiate successful oscillations. Therefore, a design trade off is established between the tuning range and the trans-conductance based on $C_f$. Moreover, $g_m$ should be maintained to a value with which oscillations can occur. However a reasonable tuning range can be obtained using the four plate Micro scale varactor. It can be concluded that by selecting suitable and optimal values for the capacitors better theoretical performance can be seen from the designed oscillator.

2. LAYOUT DESIGN

Layout of the proposed QVCO is designed using a 90nm CMOS process in Microwind environment. The CMOS section of the QVCO structure is symmetrical. The active layout area of the QVCO is 710um x 760um, including the bonding pads. The distance between the components is minimized in order to reduce the phase noise, and the layout is made as symmetrical and compact as possible to ensure differential operation and reduce parasitic inductance or capacitance.

3. SIMULATION RESULTS AND DISCUSSION

The time referenced oscillation shown in Fig 5 is generated in ADS environment using the QVCO topology. The oscillation frequency is measured as 2.40 GHz, with the variable capacitor tuning voltage $v1$ (actuation voltage of the capacitor) at 0.072 volts, and $v2$ (actuation voltage of the capacitor) at 0.9 volts. All simulations are performed with 0.6 volts power supply voltage and a current consumption of 5.8 mA in the core circuit.

![Figure 5: Output oscillations of QVCO circuit simulated using ADS](image-url)
The simulation results of phase noise using HB method with ADS is shown in Fig. 6. Since the proposed QVCO is operated under ultra low dc voltage, the cross coupled transistors are potentially biased in the weak inversion region. The phase noise is simulated as -134 dBc/Hz at an offset frequency of 1 MHz from the carrier frequency. It is noted that, for low power operations the cross coupled transistors may contribute more noise to the LC tank as the supply voltage decreases. Hence, it imposes a fundamental limitation on the phase noise of the QVCO for ultra low power and low voltage application.

Figure 6: ADS Simulated phase noise as functions of offset and noise frequency

The tested circuit is transferred to the layout for further simulation. Layout shown in Fig 4 is simulated, and the simulation results are shown from Fig 7 to Fig. 9. Fig 7 shows the simulation results when $v_1$ is varied from 0-0.3 v and $v_2$ is kept at 0.9 v. When the control voltage is increased above $V_{dd}/2$ (0.3 v) the device stops oscillating, and a dc voltage of 0.6 volts is produced as output voltage. Thus the maximum level of the control voltage is $V_{dd}/2$. Fig 8 and Fig 9 show the current waveforms of PMOS and NMOS transistors respectively. The transistors are sized to achieve the design specifications. The power consumption of the device with a supply voltage of 0.6 volts is approximately 5.8 mW. The device is simulated with a power supply voltage of 1.2 volts and the current consumption is found to be 11.9 mA. Also during the simulations it was noted that the phase noise has an inverse relation with the supply voltage. The phase noise may be improved at higher supply voltages.
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Figure 7: (a) Simulated frequency zoom view (b) Output oscillations of QVCO layout simulated using Microwind- Control voltage $v_1$ varies from 0 volts to 0.29 volts and $v_2$ is kept at 0.9 volts

Figure 8: Output voltage and current waveforms (PMOS) of QVCO layout simulated using Microwind-Control voltage varies from 0 Volts to 0.3 Volts

Table 2 shows the performance characteristics and the design variables of the QVCO. As in the table, the designed QVCO exhibits a tuning frequency range of 500 MHz, with 2.4 GHz as center frequency which leads a tuning percentage of 20.83. Because of the trade-off between the phase noise and the tuning frequency range, that the phase noise of the oscillator is inversely proportional to the tuning frequency range, the tuning frequency range is limited. The tank circuit impedance exhibits an inversely proportional relationship with the oscillation frequency.
Table 2 : Simulated results of QVCO

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Simulated Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning Range</td>
<td>20.83%</td>
</tr>
<tr>
<td>Quality factor (QVCO)</td>
<td>60 ( @ 2.4 GHz, $V_{QCONTROL}=0.56$ volts)</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>2.40 GHz</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-134 dBc/Hz @ 1 MHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>5.8 mW</td>
</tr>
<tr>
<td>Output Power</td>
<td>-8 dBm (at 50 Ω load)</td>
</tr>
<tr>
<td>Chip Size</td>
<td>710 µm x 760 µm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.6 volts</td>
</tr>
<tr>
<td>Tuning Band width</td>
<td>500 MHz (2.1 GHz-2.6 GHz)</td>
</tr>
<tr>
<td>Tank- Inductance</td>
<td>0.43 nH</td>
</tr>
<tr>
<td>Tank-Capacitance</td>
<td>10.3 pF</td>
</tr>
<tr>
<td>Tuning Voltage Range</td>
<td>0-0.3 volts</td>
</tr>
<tr>
<td>Quality factor (Resonant Circuit)</td>
<td>69</td>
</tr>
</tbody>
</table>

When the tank circuit impedance is lowered, the start-up gain gain is reduced as well as output voltage swing. Hence the value of the tank circuit impedance is carefully chosen to avoid these issues. The quality factor of the resonant circuit at 2.4 GHz is calculated as 69, which provides a quality factor of 63 for the QVCO at the same frequency. With the additional circuitry included, the quality factor of the QVCO has been predicted as 60 at 2.4 GHz. The gate-source and the drain source capacitance of the PMOS and NMOS transistors are measured between 0 to 3.5 fF.

![Output voltage and current waveforms(NMOS) of QVCO layout simulated using Microwind-Control voltage varies from 0 Volts to 0.29 Volts](image-url)
4. CONCLUSION

A 2.4 GHz QVCO is simulated and the results of the simulation are analysed. The results indicate QVCO operation at a center frequency of 2.4 GHz with a quality factor of 60. The chip size is 710 µm x 760 µm. The simulation predicts phase noise of -134 dBc/Hz at a power supply voltage of 0.6 V. The simulated oscillation amplitude is maintained slightly above V_{dd} using the feedback capacitors. The simulation operational conditions indicate that the device consumes ultra low power at 5.8 mW, including the buffer. Further the fabrication of the QVCO is expected.

REFERENCES


