ULTRA LOW-POWER DIGITAL CIRCUITS USING MULTI-THRESHOLD MTCMOS TECHNIQUE

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ABSTRACT

As various portable systems get popular, the reduction of the power dissipation in LSIs is becoming more essential. The scaling down of both the supply voltage and threshold voltage is effective in reducing the power without a serious degradation of operating speed. The static leakage current, however, enlarges the power in the sleep period when the LSI is not operating. To avoid such undesirable leakage, two methods have been reported recently. One is the "multi-threshold (MT) CMOS" which utilizes dual threshold voltages for both p- and n-channel transistors. This method, however, requires some means of holding the latched data in the sleep period which increases the design complexity and the chip area. The other is the "variable-threshold (VT) CMOS" which controls the back gate bias to increase the threshold voltage of transistors during the sleep period [3]. Although it holds the latched data, it requires a triple-well structure and an additional circuit to control the substrate bias. This work presents an in depth analysis of potential leakage paths, and yields several efficient MTCMOS flip flop implementations including a novel approach that utilizes a leakage feedback gate to enable state retention during standby modes in dynamic flip flops.

KEYWORDS: Dual Threshold Voltage, Low-Power, MTCMOS, Sub Threshold Leakage Current