HIGH-PERFORMANCE LOW-POWER SIGMA-DELTA ADC DESIGN

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ABSTRACT

The paper presents the design of high-performance low-power sigma-delta (ΣΔ) ADC suitable for micro sensors applications. High-performance means smaller delay due to low order modulator having minimum circuit elements, improved sub components specifications and low power means, the design is based on improved 180nm TSMC Mixed Mode triple well technology with small parasitic, minimum leakage, faster speed and lower high frequency effects. Since ΣΔ, Analogue-to-Digital Converters (ADCs) design takes the advantage of the improved CMOS circuit design and goes to the trend of high resolution, wide bandwidth with low-power applications having improved accuracy. Here, first order modulator has been taken in the design for equivalent performance while comparing to high order modulator due to improved design of modulator sub components and it reduces the number of mos transistors in the design while comparing to circuit complexity and other criteria in higher order modulators. Due to oversampling method, it uses high-frequency modulation and thus eliminates the need for abrupt cutoffs in the analogue anti-aliasing filters at the input to the ADCs. The detail design of its circuits were carried out using Mentor Graphics AMS Design Platform targeted to a 180nm TSMC MM triple well CMOS Technology.

KEYWORDS: Analog-to-Digital Conversion, Sigma-Delta(ΣΔ) Modulator, Decimator and Counter