EFFECTIVENESS OF MLC CAPACITORS FOR ELECTROSTATIC DISCHARGE PROTECTIONS IN AUTOMOTIVE ECUs

TAMILARASU S1, P. THIRUNAVUKKARASU2 & N. SETHUPATHI3

1Research Scholar, Bharathiar University, Coimbatore, Tamilnadu, India
2Associate Professor, Department of Electronics, SRMV College, Coimbatore, Tamilnadu, India
3Assistance Professor, Department of Physics, A. A. Government Arts College, Namakkal, Tamilnadu, India

ABSTRACT

A simple technique to deal with ESD can be achieved by mounting Multi Layer Ceramic Capacitors (MLCC) at the ECU PCB I/O connector pins which is the ESD entry point. EMC engineers recommend using 0603 MLCC’s placed at the close proximity of each connector pin, mandating low-inductance mounting strategy associated with the PCB traces and vias. When selecting SMD MLCC for ESD protection for automotive ECU I/O pins, specify the ESD capacitor value, its DC voltage rating, and a choice of technology (X7R or C0G). MLCC as an ESD bypass, or shunt device is used to divert the ESD current to ground. ESD protection devices should perform ESD mitigation and should not exhibit degradation and maintain ESD robustness throughout the life span of a product. Nevertheless, post-ESD examination of small foot-print 0603 MLCC’s reveals serious structural damage, manifesting itself electrically in a dramatic change in the impedance characteristics. This is a major departure from a pre-ESD capacitor, thus resulting in excessive low frequency leakage and functional misbehavior.

KEYWORDS: SMD MLCC, ESD Protection Devices, Electronic Control Unit (ECU)

INTRODUCTION

Electronic control unit (ECU) is a generic term for any embedded system that controls one or more of the electrical system or subsystems. In the automotive applications ECU’s are classified in to different category based on the function it does. Engine Control Module (ECM), Power train Control Module (PCM), Transmission Control Module (TCM), brake control module (BCM or EBCM), Body Control Module (BCM), suspension control module (SCM) etc are some of them. Taken together, these systems are sometimes referred to as the car's computer.

ELECTROSTATIC DISCHARGE (ESD)

Electrostatic discharge (ESD) is one of the most important reliability problems in the automotive electronic circuit industry, typically in integrated circuits used in automotive applications. One-third to one-half of all field failures are due to ESD. As ESD damage has become more prevalent in newer technologies due to the higher susceptibility of smaller circuit components, there has been a corresponding increase in efforts to understand ESD failures through modeling and analysis. Design of robust ESD circuits remains challenging because ESD failure mechanisms become more acute as critical circuit dimensions continue to shrink.

Electronics control units designers are further constrained by the ability to design highly congested PCB’s and meet ESD requirements. An ESD event is the transfer of energy between two bodies at different electrostatic potentials, either through contact or via an ionized ambient discharge (a spark). This transfer has been modeled in various standard
circuit models for testing the compliance of device targets. The models typically use a capacitor charged to a given voltage, and then some form of current-limiting resistor to transfer the energy pulse to the target.

**ESD STRESS MODELS AND TEST METHODS**

Several ESD models have been developed and standardized according to the nature of the ESD stress sources. Using these models, which are based on the physics of actual ESD events, ESD robustness of devices under different discharge processes can be characterized systematically. In reliability qualification used by the IC industry, three basic models are dominant: Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). Each of these is now summarized. One of the most frequently observed ESD events is the transfer of electrostatic charge from a charged human body to an ESD sensitive device due to improper handling. The model developed to represent this event is the Human Body Model (HBM), which is the most classical and common industrial test methods. In the HBM, it is assumed that a certain amount of electrostatic charge initially is stored on the body and the charge is transferred to an object through a finger when the physical contact between the charged human body and the object is made.

**ESD PROTECTION**

In order to meet the module level ESD tests, various methods and techniques on printed circuit boards have been implemented and investigated.

![Figure 1: ESD Protection Mechanism Used in ECU I/O Pins](image)

In this ESD protection approach, a primary ESD device exists on every I/O pad between the pad and the ground. In Figure 1, the current path for a positive discharge from the I/O pad to GND is illustrated. The ESD current flows directly from the I/O pad to GND through the ESD devices; therefore, this protection scheme is called ‘pad-based ESD protection.’ In this scheme, the primary clamp alone must hold the I/O pad voltage below the failure voltage of I/O devices in parallel.

One effective technique is to add discrete noise-decoupling components or filters into complex CMOS based IC products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test. Various types of noise filter networks can be employed to improve system-level ESD stress tests, including capacitor filters, ferrite bead, transient voltage suppressor (TVS), metal oxide varistor (MOV), and 2nd order LC filter or 3rd order π-section filters.

**MLCC OVERVIEW**

Multi layer ceramic capacitors (MLCC) are employed as an ESD bypass mechanism at the connector pins of electronic control modules. An automotive control module may require the use of a single high-density connector with pin density in excess of 200. In a typical application, a connector may present the designer with a matrix of 4 x 50 (4 rows of
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50 pins at each row) in a tightly congested PCB real estate. To accommodate for the ESD protection for each and every I/O pin at the connector of a highly congested PCB real estate, design engineers recommend the use of 0603 style MLC capacitors.

In most applications MLC capacitors used for ESD protection are rated for 100 V stress level. However, post-ESD characteristics of MLCC’s are often ignored or misunderstood. In reality, MLCC’s exposed to ESD stress exhibit dramatic shift in characteristic impedance behavior. Careful examination of MLCC’s reveals a permanent structural damage resulting in excessive low frequency leakage. Post-ESD behavior of MLCC’s results in a functional deviation for a control module and it is fundamentally unsafe to use the product for its intended application. It is suggested that the low profile 0603 capacitors should not be used for ESD protection as reported in this paper. Alternative solutions can be met by the use of low profile transient voltage suppressors (TVS) or fast metal oxide varistors (MOV). However, 0805 style MLCCs with high value capacitance (> 47 nF) provide a good solution and are safe to be used as an ESD bypass element.

MLCC’s as a protective device or mechanism should consider the voltage, peak power and energy as the key components of an ESD threat. It is thus necessary to fully characterize the amplitude and timing of ESD components. Therefore, protection structure should reduce the voltage, peak power, and energy threats by shunting the stress currents away from fragile portions of the microcontrollers and other ICs. To solve ESD problems, MLC capacitors employed as ESD bypass or filter component on printed circuit boards (PCB), must shunt the ESD transient current safely to ground. It is important that MLC capacitors employed as bypass component absorb the ESD voltage and current safely and protect the device under test with no degradation. In addition, MLC capacitor must remain within its parametric tolerance if it could be considered as a reliable protection mechanism

**MLC CAPACITOR AS AN ESD PROTECTION DEVICE**

Multi layer ceramic capacitors are designed for use where a small physical size with comparatively large electrical capacitance and high insulation resistance is required. General purpose 0603 (1.6 mm x 0.5 mm) class II, type X7R (-55°C to +125°C) is a popular choice for automotive electronic control module design. Therefore it is a common practice to apply X7R MLCC’s as ESD protection component at all I/O pins. Figure 2 illustrates a horizontal grind of 0603 MLCC (magnification X 100) with plates spaced at 21 µm apart for a 10 nF, X7R type II capacitor. A higher value capacitor is designed with increased number of plates. This will result in a narrow dielectric thickness, a possible drawback for high voltage transients. At the present time (May 2012), capacitor values for a type II X7R 0603 (100 V) range between 180 pF to a maximum value of 39 nF. However, the capacitor value range for the same technology, but larger physical size (0805), varies from 220 pF to a maximum value of 120 nF. This can be an important factor if ESD protection capacitor value is determined to exceed the maximum value of 39 nF available in 0603 package.

![Figure 2: Standard 0603 MLCC (X 100 Magnifications)](image-url)
Figure 3 illustrates inner structure of MLCC technology with respect to the design of conductive plates. Capacitor manufacturers recognize the over-voltage stress concern and have provided an ESD-enhanced MLCC product.

![Figure 3: Inner Cross Section View of 0603 MLCC](image)

Figure 4 illustrates a horizontal grind of an ‘ESD-enhanced’ MLCC on a scale of X 100 magnifications. Comparison with Figure 2 demonstrates the differences in plate geometry design. Printed circuit board designers with fundamental EMC trainings are required to ascertain the optimum mounting strategy for ESD capacitors. EMC engineers verify a “Y-Connection” topology for all of the ESD capacitors, at every I/O pin of the connector. MLCC must be placed in close proximity of the I/O pin (< 1cm) with a short trace (< 1cm) to the PCB return plane.

![Figure 4: ‘ESD-Enhanced’ 0603 MLCC](image)

In this manner, added PCB parasitic trace inductance and its degradation effect on the effectiveness of ESD bypass capacitor is minimized. The general concern is to limit the added inductance due to PCB mounting inductance, and thus provide a low-impedance path for ESD current flow to return plane.

Another limitation would be to use the lowest value capacitor available, where it is most effective at higher frequencies. ESD would result into an RF current with a bandwidth in excess of 330 MHz. The choice between a 1 nF and 680 pF would easily be reduced to the latter one. However, ESD HBM (Human Body Model) consists of a 150 pF capacitance, thus a higher value MLC capacitor is preferred. A voltage divider network is established by the combination of HBM capacitor and MLCC. The voltage developed across a larger value MLCC, would lower the voltage developed across an integrated circuit as indicated in this equation.

\[
V_{MLCC} = \frac{C_{HBM}}{C_{HBM} + C_{MLCC}} V_{ESD}
\]
Therefore $V_{MLCC} << V_{ESD}$, it is required $C_{MLCC} >> CHBM$

**SUMMARY**

This study is an examination of the physical damage to the 0603 MLC capacitors exposed to ESD transients. It is shown that permanent damage to dielectric material is resulted for ESD voltages in excess of 15 kV. The use of 0603 MLC capacitors for I/O connector pins, as an ESD bypass mechanism, is not recommended and should be avoided. However, I/O pin ESD capacitors in the range of 1 nF to 100 nF are often utilized as an input RF filter at the connector pins. The ESD capacitors provide a bypass element for the induced RF currents on the module harness due to impinging electromagnetic fields.

**REFERENCES**

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