DELAY EFFICIENT 128-BIT LADNER-FISCHER ADDER

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ABSTRACT

This paper describes the VLSI Architecture for High-Speed 128-bit Ladner-Fischer adder. The performance of Ladner-Fischer adder with black cell takes huge memory. So, the gray cell can be replaced instead of black cell that improves the Efficiency in Ladner-Fischer Adder. The three stages of operations include pre-processing stage, carry generation stage, post-processing stage. In ripple carry, adder each bit of addition need to wait for the previous bit carry. In efficient Ladner-Fischer adder, addition operation does not wait for previous bit carry since ripple carry adders are replaced by Carry select Adder (CSLA) and Binary to Excess-1 code Converter (BEC) to improve the speed and to decrease the memory used.

KEYWORDS: Ladner-Fischer Adder, Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Binary to Excess-1 Code Converter (BEC-1), Black Cell & Gray Cell

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