DESIGN AND SIMULATION OF LOW-POWER ADC USING DOUBLE-TAIL COMPARATOR

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ABSTRACT

Analog to Digital convertors (ADCs) is acts as a bridge between analog and digital components. Comparator is one of the basic & important building block of ADC circuits.

The performance of Flash Analog-to-Digital converter is affected due to Comparator and Thermometer-to- Binary encoder design. The design & simulation of 3bit analog to digital converter for low power CMOS is done using TANNER EDA Tool.

A new proposed double tail comparator is designed by adding some transistors for low power and fast operation even in small supply voltages. The encoder is design by using multiplexer which converts thermometer codes to binary codes. The circuit operates with an input frequency of 25MHz and 1.8V supply.

KEYWORDS: Low Power ADC, Flash ADC, Double-Tail Comparator, Thermometer-to, TANNER EDA Tool, Binary Encoder

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INTRODUCTION

An ADC has a bank of comparators, sampling the input signal in parallel. The comparator bank is having an encoder logic circuit that generates a code for each voltage range. Analog-to-digital converters (ADC’s) translates analog signal into digital signals. In today’s world the digitized signals are used in almost all fields. It is necessary component whenever data from the analog domain, through sensor or transducer should be digitally processed.

Figure 1: Basic ADC Circuit
For this the basic comparator operation is used. The performance of high speed analog to digital converters (ADCs) basically depends on the comparator.

The main drawback of Flash ADC is power hungry so the aim is to design low power flash type ADC with low power comparator. so our aim is to design low power comparator and encoder.

In this paper, we have designed the low power flash ADC for the optimization of power performance. so for that design consist of resistive ladder, series of comparator and encoder. Comparator is Double-tail comparator that operate faster and can be used in lower supply voltages. the Thermometer to Binary code converter which is the multiplexer based encoder. The design is done in Tanner EDA tool.

SYSTEM ANALYSIS

Problem Definition

Analog-to-digital converters (ADC’s) converts analog signal into digital signals, for data transmission and control systems. ADC consist of resistor ladder, bank of comparator and encoder. The performance of high speed analog to digital converters (ADCs) basically depends on the comparator. At time of conversion of analog to digital form mostly involves comparator action where the value of analog voltage at some point in time is compared with some standard value. Comparator is one of the building blocks in most of the analog-to-digital converters with which the process of data conversion take place. Many high speed ADCs, such as flash ADCs, SAR ADCs require high-speed, low-power comparator.

Proposed System Feature

FLASH ADC

Flash ADC is having another name i.e. the parallel A/D converter, this circuit is the simplest to understand. It is formed of a bank of comparators, each one comparing the input signal to a one reference voltage. The comparator outputs connect to the inputs of a 8-line to 3-line priority encoder circuit, which then produces a binary output. The following block diagram shows a 3-bit flash ADC circuit:

![Diagram of a 3 Bit Flash Type ADC](image)

Figure 2: Circuit Diagram of a 3 Bit Flash Type ADC

The working of Flash Analog-to-Digital converter is depends on the choice of Comparator and Thermometer-to-Binary encoder design. The design & simulation of 3bit and an 4bit analog to digital converter for low power CMOS is done using TANNER EDA Tool. It requires 2N-1 comparators, an encoder to convert thermometer code to binary code.
This ADC design uses double-tail comparator circuit for the reduction of power and the comparator circuit is simply modified. The design and Pre simulation are carried out in tanner EDA tool using simulator under 250nm technology.

**Comparator**

Comparator is building blocks of the analog-to-digital converters which converts data conversion. Many high speed ADCs, such as flash, SAR ADCs, require high-speed, low-power comparator.

The designing of double tail comparator has dual input, dual output that is suitable for high speed analog-to-digital converters. The double tail comparator also has low voltage and power.

**SYSTEM DESIGN AND IMPLEMENTATION**

**Proposed Structure Double-Tail Dynamic Comparator**

Figure 3: Schematic Diagram of the Dynamic Double-Tail Comparator

Figure 4: Operation of Comparator

Figure demonstrates the schematic diagram of the dynamic double-tail comparator. Due to the better performance of double-tail design in low-voltage applications, the proposed comparator is designed based on the double-tail structure.[1]
The conventional double tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference, in the proposed design as soon as the comparator detects that for node fn discharges faster, a pMOS transistor turns on, pull back the other node fp to the Vdd. Therefore after some time, the difference between fn and fp ($\Delta V_{fn/fp}$) increases exponentially, leading to the reduction of latch regeneration time. So working of comparator, one of the points which should be considered is that in this circuit, when one of the control transistors is turn on, a current from Vdd is drawn to the ground via input and tail transistor, resulting in static power consumption. To overcome this issue, four nMOS switches are used below the input transistors such as Msw1, Msw2, Msw3 and Msw4.

![Figure 5: Schematic of Double Tail Comparator in Tanner EDA Tool](image)

**Thermometer to Binary Code Converter**

For 3bit ADC, the logic encoder used is as shown in figure. This is a multiplexer based encoder which converts thermometer codes to binary codes. The multiplexers used are designed using transmission gates for well accuracy.[2]

![Figure 6: Logical Diagram of 3-Bit Encoder](image)
Table 1: Truth Table for 3bit Encoder

<table>
<thead>
<tr>
<th>C7</th>
<th>C6</th>
<th>C5</th>
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Figure 7: Schematic View of Logical Encoder of 3 Bit ADC in Tanner EDA Tool

Figure 8: Schematic Of 3-Bit ADC In Tanner EDA Tool
RESULTS

Figure 9: Waveform of Working of Double Tail Comparator

Figure 10: Waveform of Working of Logical Encoder

Figure 11: Waveform of Working of 3-Bit ADC
Table 2: Power Values of Different Circuits in Tanner EDA Tool

<table>
<thead>
<tr>
<th>Design</th>
<th>Power</th>
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<tbody>
<tr>
<td>Double-tail Comparator</td>
<td>0.0169mW</td>
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<tr>
<td>Thermometer-code Convertor Encoder</td>
<td>0.6512µW</td>
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<tr>
<td>3-Bit Flash ADC</td>
<td>0.283mW</td>
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CONCLUSIONS

- In this paper, we have examine the design and simulation of low power ADC using double tail comparator. The design and Pre simulation are carried out in tanner EDA tool using simulator under 250nm technology.
- The circuit operates with an input frequency of 25MHz and 1.8V supply for ADC. The Average power of 3-bit ADC is about 0.283mW.
- The ADC design can be used for low power and high speed applications. The proposed architecture can be extended to higher resolution.

REFERENCES
