DESIGN ANALYSIS AND COMPARATIVE STUDY OF RF RECEIVER FRONT-ENDS IN 0.18-µM CMOS

M. Sumathi[1] **and S. Malarvizhi**[2]

[1] *Research Scholar, Department of ECE, Sathyabama University, Chennai-119, India*
sumana_gopi@yahoo.co.in
[2] *Professor/ Head of the Department, ECE, SRM University, Kattankulathur, India*

ABSTRACT

In this work, design and simulation results of two RF front-ends to be used in direct conversion receiver are presented. The first one uses dual CS differential LNA with folded mixer. The second one uses single-ended LNA with double balanced mixer. Single-ended and fully differential LNA's provide gains of 16.3 dB and 28.75 dB at 2.4GHz, respectively. Noise Figure of these two LNA's are 3.34 dB and 2.7 dB. The differential LNA merged inductor based folded mixer provides a conversion gain of 13dB with a noise figure of 7.9dB at 150MHz IF. Similarly, the single-ended LNA merged double balanced mixer provides a conversion gain of 9dB with a noise figure of 10dB. These results are obtained from 1.8V supply and design evaluations are realized using 0.18-µm CMOS technology scale. The design principles, advantages, limitations and performance comparison are highlighted.

Keywords: *CMOS,Direct Conversion, Front-end ,LNA,Mixer,Radio Frequency(RF).*

1. INTRODUCTION

Today the RF research trend moving towards the implementation of RF wireless products using deep-submicron CMOS technologies. It allows the operation frequency of CMOS circuits above 1GHz, and makes the possibility for realization of integrated RF CMOS circuitries or systems. Because of the digital revolution and higher growth of portable wireless devices market require many

changes to the analog front-ends. It is of need to find newly innovative design circuitries for these front-ends. Basically, front-ends are responsible for tracking weak signals (RF) at high frequency and translating into IF signals for transmitting with high power levels. It is an interface between the antennas and digital modem of the wireless transceiver. Therefore, it needs high performance analog circuits like LNA's and Mixers. The following are the existing receiver topologies such as Zero-IF, Heterodyne, Low-IF and wide-band IF in RF transceivers. Recent research works proved that Zero-IF always the popular and widely used for RF applications, [1] among these four architectures. This is due to the possibility of higher degree of integration, lesser power dissipation and lesser off-chip components. The block diagram of the direct conversion RF front-end designed in this paper is illustrated in Fig.1. RF amplification and Down-Conversion stages are the most important requirement of the system performance and also the challenging design implementations in CMOS. Another criteria is supplying power to the circuits that relates Battery technology which does not improve as the electronics technology improved. It is an important demand to introduce new designs which should be suitable for low voltage applications.

Many short range receiver front-end circuits such as LNA's and Mixers have been published[4]-[10],but with a higher supply voltage and technology scale. In this work, the design ideas and performance of two 2.4GHz front-ends have been explored. The front-end 1 used with single-ended LNA and double-balanced mixer. The front-end 2 built with differential LNA and inductor based mixer. The problems and possibilities of merging LNA's and Mixers highlighted in time domain and frequency domain results. The complete work is organized as follows. Section II presents design of single-ended LNA and differential LNA. Section III describes the design of mixers and front-ends in detail. The simulated results are shown and performance comparison discussed in section IV.
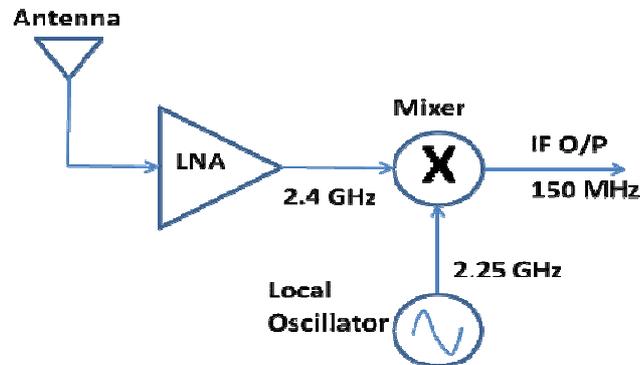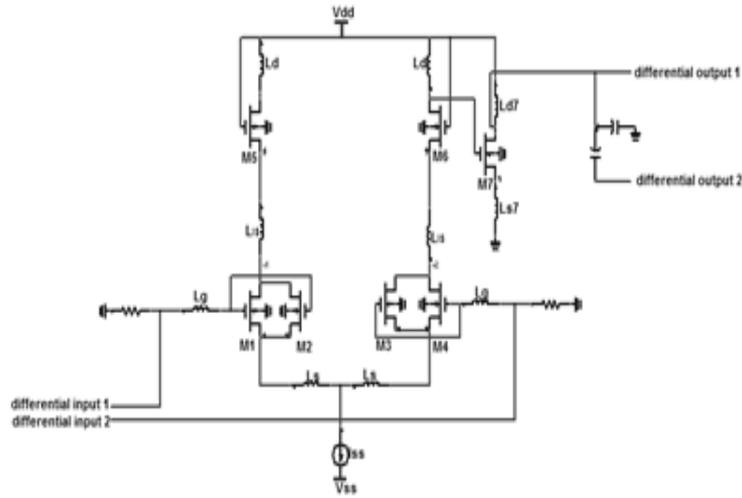
Figure. 1. Block diagram of Receiver front-end

2. LNA DESIGN

It is necessary to revise the existing and re-evaluate the topologies of LNA which is an important block in the receiver front-end whose function is to amplify the received input signal and to overcome the noise generated in the following stages of the system. In this paper, the circuit design is evaluated in single-ended and differential topology. The proposed LNA topologies are shown in fig.4. and fig.5.The Cascode structure is the one, commonly used in LNA. It is composed of common source and common gate (CS-CG) stages. The proposed single-ended LNA uses dual CS transistors M1, M2 in CS stage. The modified cascode structure is shown in Fig.2.Two nMOS transistors M1, M2 are connected in parallel for each CS stage. Therefore, the gate-source capacitances and device currents are paralleled in the equivalent circuit model, shown in Fig.3. An inter-stage matching inductor is placed in between CS & CG stages for betterment of impedance matching and gain. Transistor M1 and M2, gate inductance L_g and source inductance L_s are responsible for input impedance and the gain required. Transistor M3 and L_D provide the output impedance required. Another LNA is differential cascode narrowband with inductive source degeneration. Two single-ended LNA stages are combined together to built a differential LNA. The first stage provides the input impedance and the gain

required and is conformed by the transistor M1, the gate inductance L_g and the source inductance L_s and vice-versa. L_d, R_d and C_d are responsible for output impedance matching network. In dual CS stage, transistor M2 size was chosen approximately equal to M1 size. Source degeneration provides real input impedance for specific frequency without noise.

Figure 2. Single CS stage using two transistors

Figure 3. Equivalent circuit for input stage of LNA

Figure 4. Proposed CMOS Single ended LNA

Figure 5. Proposed CMOS Differential LNA

The following LNA topology characteristics are an essential for LNA performance which may be single-ended or differential type and derived from equivalent circuit for input stage of LNA is shown in fig.3. The input impedance at resonant frequency is expressed as,

$$Z_{in} \quad {}_T L_s \tag{1}$$

where ω_T is the cut-off frequency, expressed in terms of transconductance and gate to source capacitance shown in eqn.(2) for modified CS stage or dual CS stage.

$$_T \quad \frac{(g_{m1} \quad g_{m2})}{C_{gs1} \quad C_{gs2}} \tag{2}$$

g_m and C_{gs} were chosen to ensure impedance matching of 50 ohms and resonance at 2.4GHz. L_s is the source inductance selected between 0.5 to 1nH.The Q of an inductor determined from technology parameters and its value

lies between 6 to 10. The gate inductance L_g determined from Quality factor Q, source impedance R_s and desired frequency f_o and shown in eqn.(2).

$$L_g = \frac{QR_s}{2\pi f_o} \tag{3}$$

From these two values of L_g and L_s, the gate to source capacitance can be derived by using this eqn.(4)

$$\omega^2_o = \frac{1}{C_{gs}(L_g + L_s)} \tag{4}$$

C_{gs} is related with oxide specific capacitance C_{ox}, whose value is calculated by using eqn.(4)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{5}$$

where ε_{ox} is the permittivity of oxide layer and t_{ox} is the thickness of oxide layer whose value is 4.1nm in 0.18-µm CMOS technology. The drain inductance value is evaluated from this fundamental eqn.(5). where f_o is equal to 2.4GHz and C_{out} lies between 0.6pF to 1pF.

$$f_o = \frac{1}{2\pi\sqrt{L_d C_{out}}} \tag{6}$$

The bias transistor M4 width is approximately equal to one fourth of the CS transistor. Finally, the optimized width of TSMC RF nMOS transistors are calculated with the help of channel length (L) , gate to source capacitance and oxide capacitance and it is given in eqn.(6).

$$W \quad \frac{4C_{gs}L}{3C_{ox}} \tag{7}$$

3. MIXER DESIGN

A mixer is a frequency translator which converts RF signal into IF signal. The following are the basic building stages of a mixer that is RF transconductance stage, LO switching stage and output load resistor stage. In a mixer design, Gilbert mixer is the most popular double balanced mixer and widely used in RFIC designs. The proposed mixer designs developed for low voltage applications. There are two modifications done here, one in transconductance stage, another in biasing. The RF stages are completely revised in both designs. In order to utilize the low supply voltage both RF and LO stages have been biased separately and it is done with passive elements such as resistors. The first design uses inductors at RF input stage for providing better impedance matching and reducing noise figure and the second one uses series form of transistors. Both architectures are shown in front-end designs. The first design is, double balanced, inductor based down-conversion mixer comprises differential pair RF transconductance stage (M5-M6), four differential switching quads (M1-M4) and load resistors (R1, R2). R3 and R4 are the biasing resistors of the transconductance stage. Inter-stage Inductor L is placed between the RF and LO stages. L_g and L_s inductors used for the input impedance matching at 50 ohm. Therefore, only current through the RF stage increased, but allows smaller LO drive voltage and improves the entire performance. The second design mixer uses series form of transistors (M5-M8) in RF transconductance stage, four switching quads (M1-M4) and load resistors. The design values for the transistors and other circuit elements for both the mixers are evaluated as follows, The W/L ratio of the transistors are determined from transconductance (g_m), shown in eqn.(8). and eqn.(9).

$$g_m \quad [\frac{4R_L}{A_V} \quad R_s]^{-1} \tag{8}$$

$$\frac{W}{L} \quad \frac{g_m^2}{4KI_{ds}} \tag{9}$$

where R_L , R_s represents the load and source impedances. A_V , K and I_{ds} represents the voltage gain ,process dependent term and drain-source current flowing to the load. The widths of the transistors are approximately lies between 50 to 70µ m.

4. FRONT-END DESIGN AND ANALYSIS

The proposed front-ends are shown in fig.6 & fig.7. The front-end 1 consists of a differential LNA followed by an inter stage inductor based mixer. The mixer is loaded by the output impedance of the LNA. The front-end 2 consists of a single-ended LNA followed by a double-balanced mixer. The single-ended LNA Mixer Interface done with the help of baluns which are used to provide differential into single transformation IF output signals. The front-end is mainly characterized for conversion gain and noise figure performance.
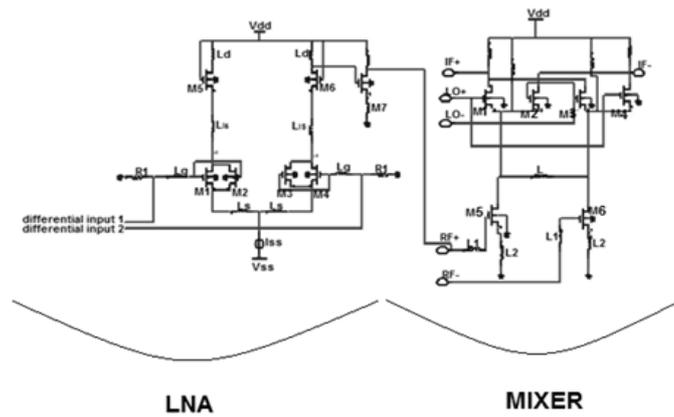
Figure 6. Proposed Front-end 1
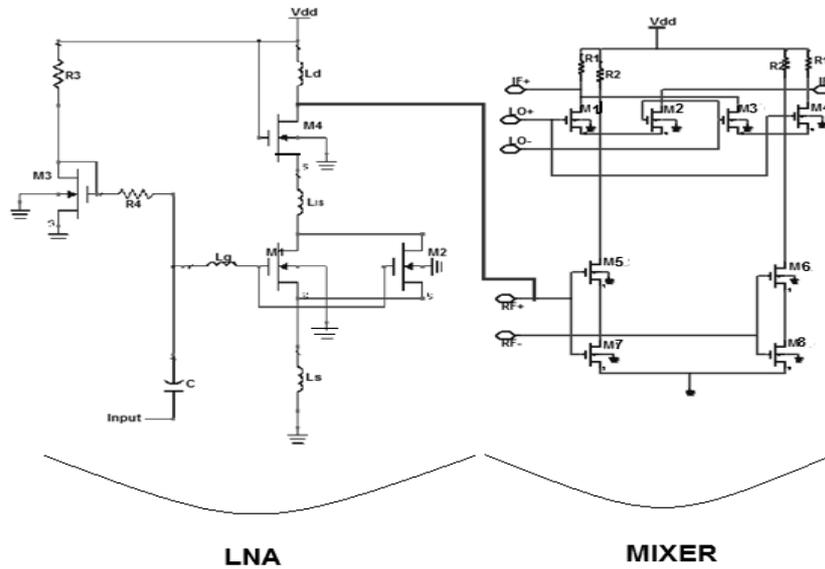
Figure 7. Proposed Front-end 2

## 5. SIMULATION RESULTS

The simulations of the front-ends are based on TSMC 0.18-µ m CMOS RF models. Agilent's Advanced Design System (version 9.0) EDA tools used to evaluate the performances of these circuitry designs. The proposed front-end operated at RF frequency of 2.4GHz, LO frequency of 2.25GHz and IF frequency of 150MHz. The input impedance matching and forward gain of Differential LNA analysed by S-parameter test and shown in Fig.9 and Fig.8. The conversion gain and noise figure of the front-end 1 are measured and shown in Fig.10 &11, while sweeping LO power at 5dBm.
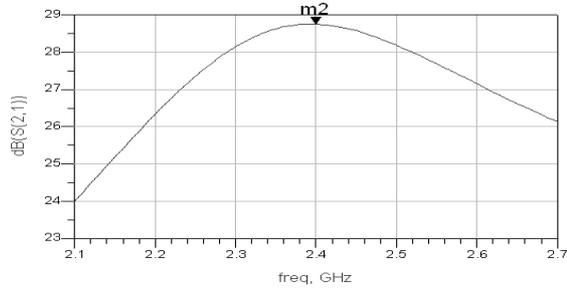
Figure 8. Forward gain of Differential LNA

The LNA input impedance matching and maximum voltage gain values at 2.4GHz RF frequency are -8.5dB, 28.75dB respectively.   Both input /output impedance matching are satisfied well for 2.4GHz design constraints. The peak conversion gain is about 13dB and noise figure of 7.9dB indicated by markers m1 and m2.
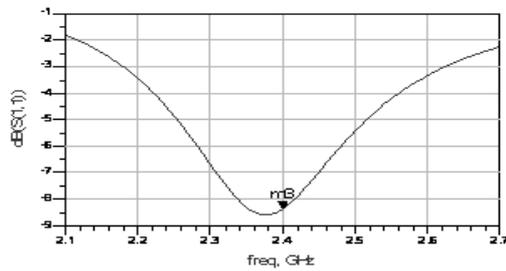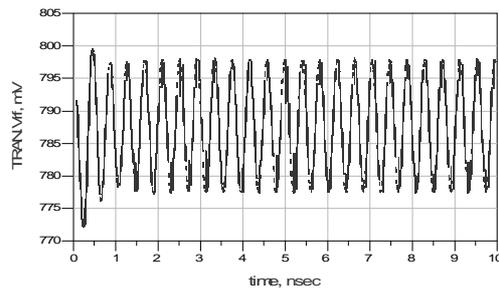

Figure 9. Differential LNA impedance matching1
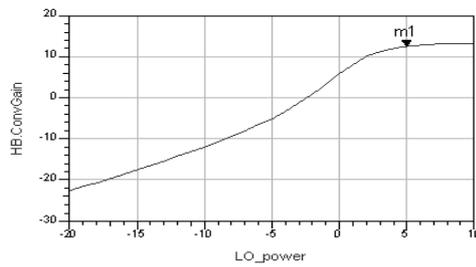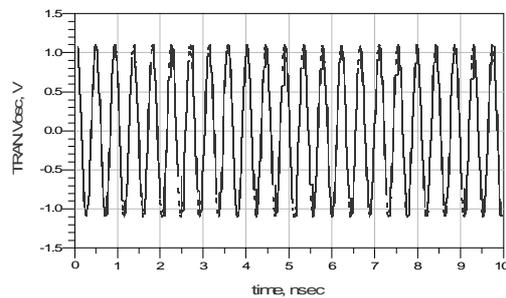

Figure 10. Conversion Gain of Front-end 1
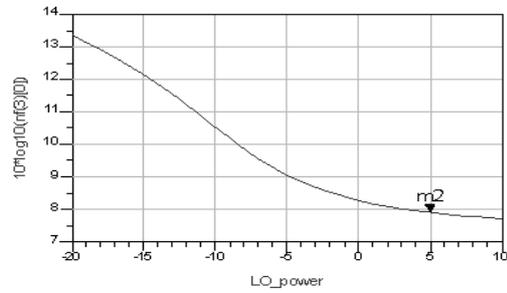
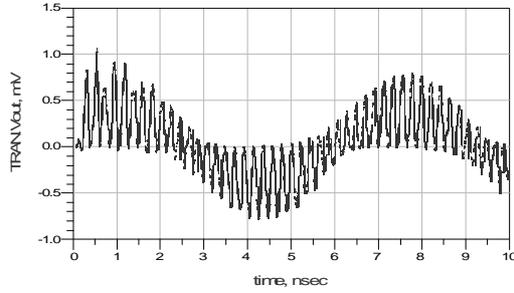**Figure 11. Noise Figure of Front-end 1**

The simulated waveforms of RF, LO and IF signals are represented with respect to time and it is shown in fig.12, 13& 14. The IF spectrum output is shown in fig.15. that indicates IF frequency 150MHz.
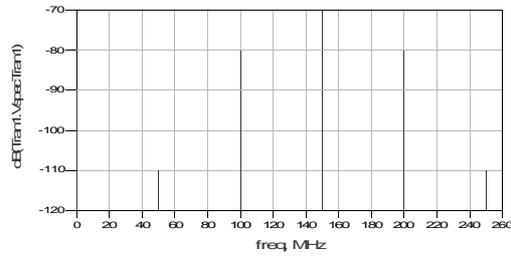

Figure 12. Simulated RF signal

Figure 13. Simulated LO signal

Figure 14. Simulated IF signal

Figure 15. Simulated IF spectrum

The single ended LNA achieves a power gain of 16.75dB, 3.35dB noise figure at 2.45GHz, shown in fig.16&17. Fig.18 shows the conversion gain of front-end 2 as a function of the differential LO power. By sweeping the LO power from -30dBm to +10 dBm, both conversion gain and noise figure are simulated and it is shown in fig.18 & fig.19 . The RF signal power is set to be 30dBm. The conversion gain is about 9dB and noise figure is about 10dB when LO power is 5dBm. There are many parasitic effects exist in RF design while analyzing the performance particularly at high frequency and therefore the original TSMC foundry RF CMOS model is provided to get optimized results.
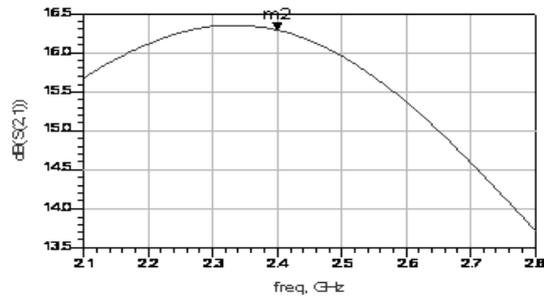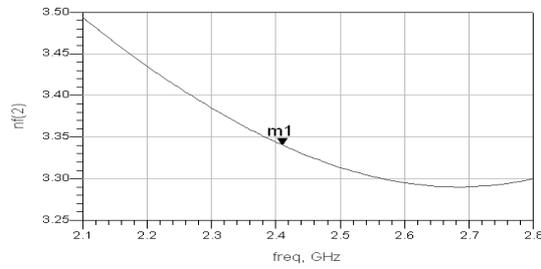
Figure 16. Forward gain of Single ended LNA

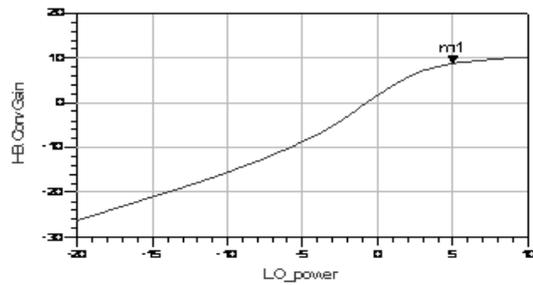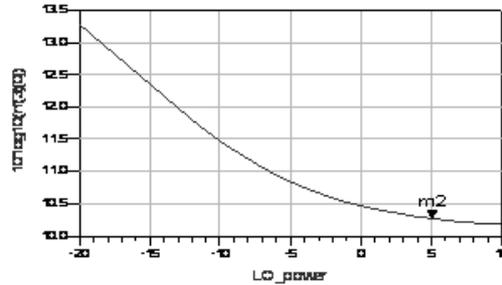
Figure 17. Noise Figure of Single-ended LNA

Figure 18. Conversion Gain of Front-end 2

Figure 19. Noise Figure of Front-end 2

Table 1. shows the performance comparison of front-ends with recently published designs. The results are comparably better for Front-end1 and suitable for low voltage applications.   This possibility made due to the superior performance of differential LNA and its differential topology while interfacing with inductor based mixer.

Table 1. Performance Comparison

Front-end	Tech.(µm)	Freq.(GHz)	CG(dB)	NF(dB)
[6]	0.18	2.4	11	14
[9]	0.18	2.4	23	8.1
Front-end1	0.18	2.4	13	7.9
Front-end2	0.18	2.4	9	10

5. CONCLUSIONS

In this paper, two front-ends suitable for direct-conversion receivers have been proposed. The design and performance of these front-ends are analysed in a TSMC 0.18-µm CMOS technology scale with 1.8V supply. It operates at 2.4GHz and converts the IF frequency of 150 MHz by mixing with the LO frequency of 2.25GHz. The front-end1 provides a gain of 13dB with a noise figure of 7.9dB. The front-end 2 provides a gain of 9dB with a noise figure of 10dB. From this study, the performance of differential LNA is better than single-

ended LNA with mixer interface and helps to improve the overall performance of the front-end. Due to these highly linear performance front-end blocks, the linearity of the overall receiver system can also be improved.

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