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MODELLING OF TOWERING SPEED AND AREA COMPETENT VEDIC MULTIPLIER

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ABSTRACT

High speed pipelined multiplier architecture is proposed in this paper. The pipelined architecture consists of 3 stages. 1st stage consists of the 4 - bit Vedic Multiplication unit. 2nd stage consists of partial products and carry. 3rd stage consists of adders and the result of the multiplication. This paper presents the efficiency of Urdhva Tiryakbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates complex multiplication steps. The proposed algorithm is modeled using VHDL, a hardware description language. It is found that 11 logic cells are required to build nibble multiplier. The propagation time of the proposed architecture is found to be 4.585ns. Implementation has been done for the Xilinx FPGA device, Spartan-3E. The layout is designed by using Microwind. The results shows that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures.

KEYWORDS: Vedic Mathematics, Urdhva Triyakbhyam Sutra, Array Multiplier, Booth Multiplier, Nibble, High Speed

INTRODUCTION

Multiplier [1] is one of the key hardware blocks in designing arithmetic, signal and image processors. Many transform Algorithms like Fast Fourier transforms (FFTs), DFT etc make use of multipliers [2], [3], [4]. With advances in technology, many researchers have tried to design multipliers which offer high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier.

In recent years, high-speed multipliers [5] play an important role while designing any architecture and researchers are still working on many factors to increase the speed of operation of these basic elements. Algorithms for designing high-speed multipliers have been modified and developed for better efficiency [6]. The increased complexity of various applications, demands not only faster multiplier chips but also smarter and efficient multiplying algorithms that can be implemented in the chips. It is up to the need of the hour and the application on to which the multiplier is implemented and what tradeoffs need to be considered. Generally, the efficiency of the multipliers are classified based on the variation in speed, area and configuration.

The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial-parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers. The proposed Vedic multiplier is based on the Vedic Sutras. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware.

VEDIC MATHEMATICS

The Sanskrit word *'Veda'* means *'knowledge*'. The Vedas consist of a huge number of documents there are said to be thousands of such documents in India, many of which have not yet been translated, which are shown to be highly structured, both within themselves and in relation to each other. Some documents, called *'Ganita sutras'* (the name 'Ganita' means Mathematics), were devoted to mathematical knowledge. Sri Bharati Krishna Tirtha Maharaj, who is generally considered the doyen of this discipline, in his seminal book *Vedic Mathematics* wrote about this special use of *sutras [11]*. Vedic Mathematics" was the name given by him. He was the person who collected lost formulae from the writings of "Atharwa Vedas" and wrote them in the form of Sixteen Sutras and thirteen sub-sutras. Vedic Mathematics is based on 16 sutras dealing with mathematics related to arithmetic, algebra, and geometry. These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus and applied mathematics of various kinds. The Vedic methods are direct, and truly extraordinary in their efficiency and simplicity. Research is being carried out in many areas, including the effects on children who learn Vedic maths and the development of new, powerful but easy applications of the Vedic sutras in geometry, calculus, computing etc. But the real beauty and effectiveness of Vedic mathematics cannot be fully appreciated without actually practising the system. One can then see that it is perhaps the most refined and efficient mathematical system possible.

Vedic Mathematics Sutras

This list of sutra is taken from the book Vedic Mathematics, which includes a full list of the 16 main sutras. The following are the 16 main sutras or formulae of Vedic math and their meaning in English.

- (Anurupye) Shunyamanyat - If one is in ratio, the other is zero
- Chalana-Kalanabyham - Differences and Similarities.
- Ekadhikina Purvena - By one more than the previous one.
- Ekanyunena Purvena - By one less than the previous one
- Gunakasamuchyah - The factors of the sum is equal to the sum of the factors
- Gunitasamuchyah - The product of the sum is equal to the sum of the product
- Nikhilam Navatashcaramam Dashatah - All from 9 and the last from 10
- Paraavartya Yojayet - Transpose and adjust.
- Puranapuranabyham By the completion or noncompletion
- Sankalana-vyavakalanabhyam - By addition and by subtraction
- Shesanyankena Charamena - The remainders by the last digit
- Shunyam Saamyasamuccaye - When the sum is the same that sum is zero
- Sopaantyadvayamantyam - The ultimate and twice the penultimate
- Urdhva-tiryakbyham - Vertically and crosswise
- Vyashtisamanstih - Part and Whole
- Yaavadunam - Whatever the extent of its deficiency

URDHVA TIRYAKBHYAM SUTRA

The Multiplier Architecture is based on the Vertical and Crosswise algorithm [7], [8]. The architecture is illustrated with two 4-bit numbers; the multiplier and multiplicand, each are grouped as 4-bit numbers so that it decomposes into 4x4 multiplication modules. After decomposition, vertical and crosswise algorithm is applied to carry out the multiplication on first 4x4 multiply modules. The results of first 4x4 multiplication module are utilized after getting the partial product bits parallel from the subsequent module to generate the final 16-bit product. Hence any complex NxN multiplication can be efficiently implemented by using small 4x4 multiplier using the proposed architecture where N is a multiple of 4 such as 8 , 16, ...2N. Therefore efficient multiplication algorithm implementation with small numbers such as 4-bits can be easily extended and embedded for implementing efficient NxN multiply operation.

The proposed method of Urdhva Triyagbhyam can be implemented for binary system in the same way as decimal system.

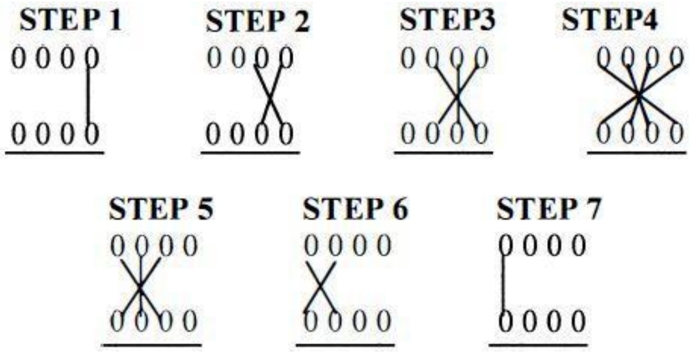

Figure 1: Example of 4x4 Binary Multiplication Using Urdhva Tiryakbhyam

The 4 x 4 multiplication has been done in a single line in Urdhva method, whereas in shift and add method (Conventional) four partial products have to be added to get the result. This implies the increase in speed. Urdhva Tiryakbhyam (Vertically and Crosswise), deals with the multiplication of numbers [8], [9], [12]. This Sutra has been traditionally used for the multiplication of two numbers in the decimal number system. In this paper, we apply the same idea to the binary number system to make it compatible with the digital hardware [10]. Let us first illustrate this Sutra with the help of an example in which two decimal numbers are multiplied. Line diagram for the multiplication of two numbers (325x728) is shown in Figure. 2. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be zero.

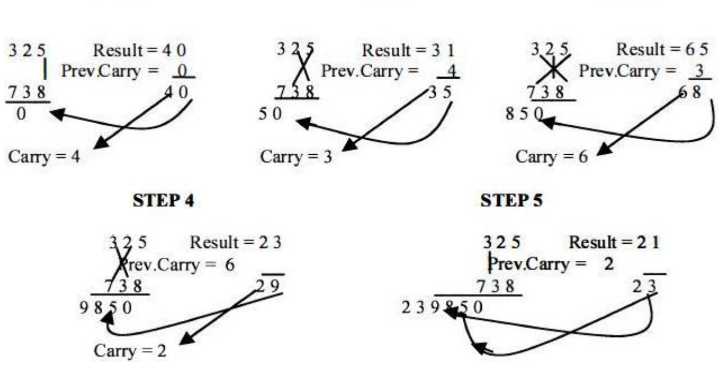

Figure 2: Multiplication of Two Decimal Numberss by Urdhva Tiryakbhyam

We now extend this Vedic multiplication algorithm to binary number system with the preliminary knowledge that the multiplication of two bits a0 and b0 is just an AND operation and can be implemented using simple AND gate. To illustrate this multiplication scheme in binary number system, let us consider the multiplication of two binary numbers a3a2ala0 and b3b2blb0. As the result of this multiplication would be more than 4 bits, we express it as ... r3r2r1r0. Line diagram for multiplication of two 4-bit numbers is shown in Figure. 1 which is nothing but the mapping of the Figure. 2 in binary system. Thus we get the following expressions:

$$r0 = a0b0, \tag{1}$$

$$c1r1 = a1b0+a0b1, \tag{2}$$

$$c2r2 = c1+a2b0+a1b1+a0b2, \tag{3}$$

$$c3r3 = c2+a3b0+a2b1+a1b2+a0b3, \tag{4}$$

$$c4r4 = c3+a3b1+a2b2+a1b3, \tag{5}$$

$$c5r5 = c4+a3b2+a2b3, \tag{6}$$

$$c6r6 = c5+a3b3, \tag{7}$$

With c6r6r5r4r3r2rlr0 being the final product. Partial products are calculated in parallel and hence the delay involved is just the time it takes for the signal to propagate through the gates.

HARDWARE ARCHITECTURE

The main advantage of the vedic multiplication algorithm (Urdhva-Tiryak Sutra) stems from the fact that it can be easily realized in hardware. The hardware realization of a 4-bit multiplier using this Sutra is shown in Figure. 3. This hardware design is very similar to that of the famous array multiplier where an array of adders is required to arrive at the final product. All the partial products are calculated in parallel and the delay associated is mainly the time taken by the carry to propagate through the adders which form the multiplication array.

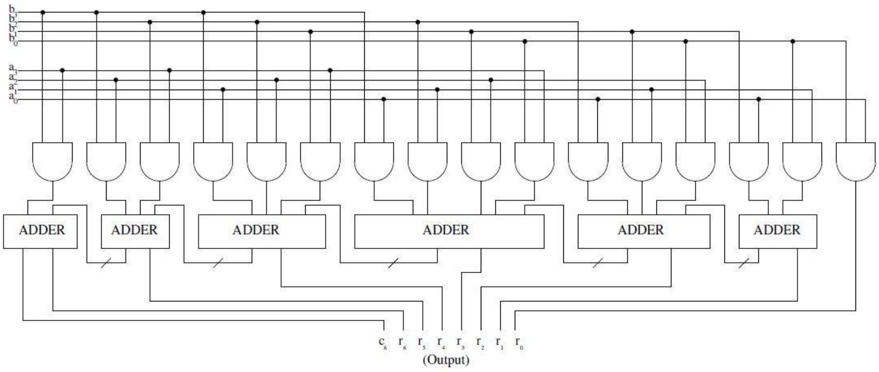

Figure 3: Hardware Architecture of the Proposed Vedic Multiplier

IMPLEMENTATION OF VEDIC MULTIPLIER

The Proposed Algorithm

The pseudo code of the proposed multiplication algorithm is described. The algorithm is broadly divided in three stages namely the initialization, pre-processing and processing.

The proposed multiplication algorithm is for n-bit multiplication using basic shifting, multiplication and addition operations.

Pseudo Code

Initialization

```
    Positive edge clock (elk) and negative edge reset (rst_n) is initialized.
    Reg [n-2:0] = 0. (Temporary Registers)
    P [n-l :0] = 0. (Partial Products)
    Cy [n-3:0] = 0. (Carry)
    Load enable (Iden) = 0.
    Operation enable (open) = 0.
```

Pre-Processing

```
    Input n-bit binary numbers a and b
    a[n-l :0] = Multiplicand
    b[n-l :0] = Multiplier
    Load Enable (Iden) = 1.
    Operation enable (open) = 0.
    temp_b [n-l:0] = Right shift of b.
```

Processing

```
    Operation enable (open) =0.
•   Right shift the multiplier b [n-l :0] n*2 times.
•   Multiply a and b w r t expressions.
•   Add [n-2:0] = {p (0) + P (1) + ... + P (n-2) + p (n-l)} + cy(n-3:0).
•   Result = right shift add [n-(4*multiple of 4)] n*2 times.
•   Return the result.
•   END.
```

Analysis of the Algorithm

Basic multiplication unit used is nibble multiplication. The computer architecture designed such a way that nibble, byte, word, etc., are used to perform basic operations. Hence the same concept is applied to develop the multiplication algorithm using vedic sutras. In our algorithm, we consider nibble as leaf cell for the higher bit multiplications design.

The proposed multiplication algorithm is hierarchical in structure i.e., top-down approach. Thus, using basic nibble multiplication unit, the higher bit multiplication can be built which will makes modification easier. Hence debugging is easy and efficient in area and speed. In the conventional method, for n-bit multiplication n*4 AND gates are used for implementation. The proposed multiplication algorithm uses n AND gates for n-bit multiplication. Thus, area consumption is less. The method uses sequential circuits in the design that used for different frequency ranges. Speed is increased by reducing the delay in sequential circuits.

The above figure shows proposed way of nibble multiplication by Urdhva Tiryakbhyam Sutra. For the case, nibble multiplication of a [3:0] and b[3:0]. The analysis is as follows. It takes n*2 clock cycles for n-bit multiplication. In nibble multiplication 8 clock cycles are required to get the result. In the 151 clock cycle, a[0] is multiplied with b[0] and a[l], a[2], a[3] are multiplied with reg[0], reg[l], reg[2] respectively.

After getting the partial products p[3:0], added with carry using simple adder. The add [0] is feed to the result and add[2: 1] acts as carry. For next clock cycles, b[3:0] is right shifted by 1 bit and multiplied with corresponding a[3:0] bits. Then partial products are added with previous carry using simple adder and add [0] is feed to the result and previous addition result is right shifted by 1 bit. Likewise, for each clock cycle the method follows. After 7th clock cycle result is generated and stored in 8 bit register.

EXPERIMENTAL RESULTS

The algorithm is designed for 4 bit input using VHDL-HDL. Simulation is done using Xilinx 9.1. Synthesis and Implementation is done using Xilinx Spartan-3E FPGA Board of device family xc3s500e-4fg320. The layout is designed by using Microwind.

The subsequent figures show the simulation, Technical Schematic and Layout of nibble multiplication. The simulation and synthesis results for the Vedic, Array and Booth multipliers are respectively shown below.

Vedic Multiplier

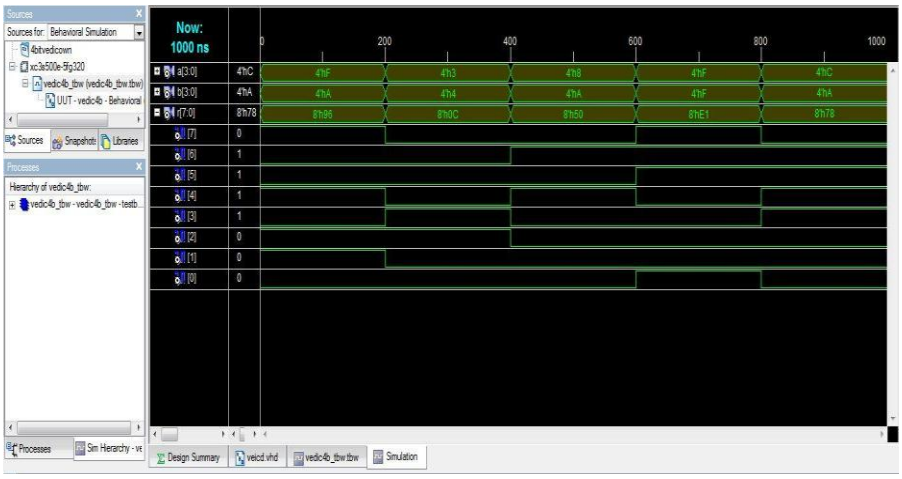

Figure 4: Simulation Results for 4-Bit Vedic Multiplier

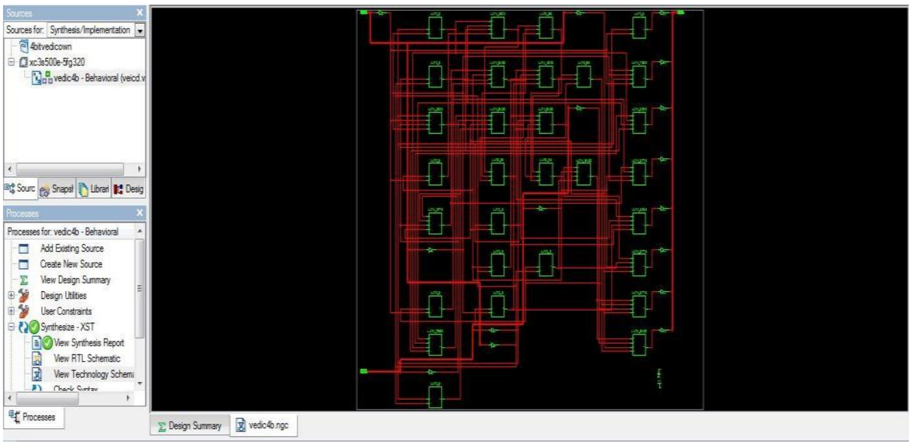

Figure 5: Technology View of 4-Bit Multiplier Using Vedic Mathematics

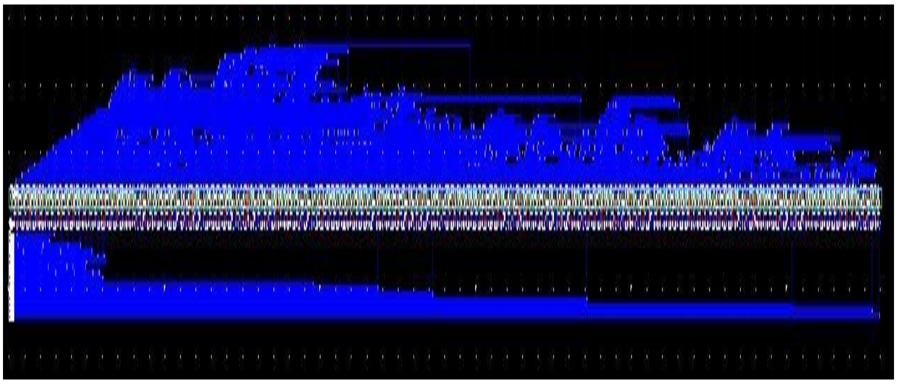

Figure 6: Layout Diagram of 4-Bit Vedic Multiplier

Array Multiplier

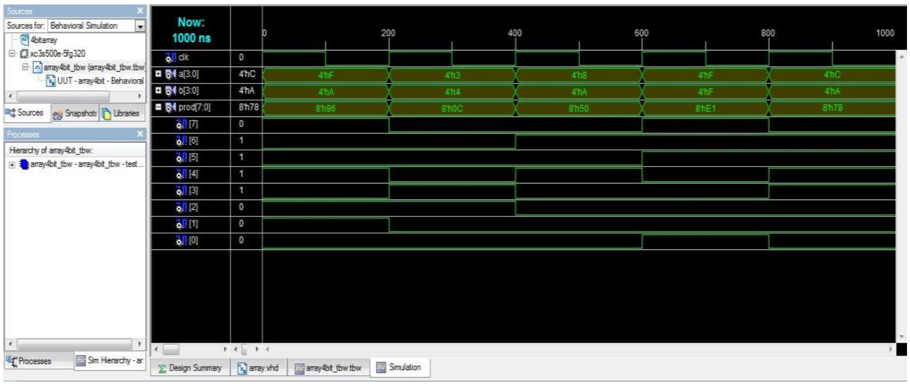

Figure 7: Simulation Results for 4-Bit Array Multiplier

Booth Multiplier

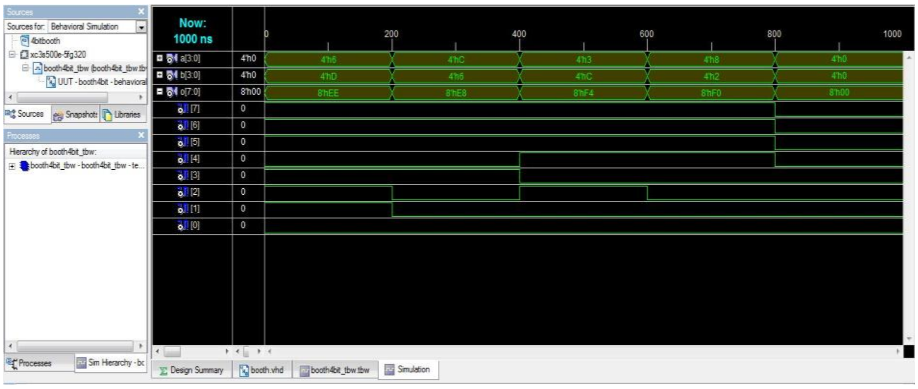

Figure 8: Simulation Results for 4-Bit Booth Multiplier

The area consumed and speed taken to do the implementation for 4-bit Vedic, Booth and Array multipliers are given in below Charts.

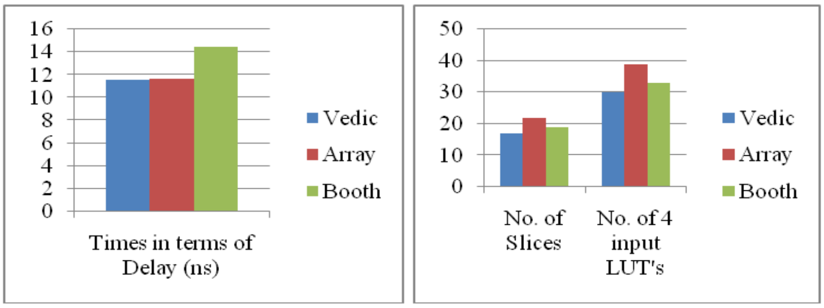

Figure 9: Comparison of 4-Bit Multipliers with Respect to Delay and Area in Spartan 3E FPGA

CONCLUSIONS

The Delay of the proposed Vedic multiplier is 4.585ns. Hence, the maximum operating frequency of the proposed multiplier is found to be 218.103MHz under normal operating conditions and with all the input signals having normal inputs. It is evident from the summary that only 11 logic elements are required for the proposed Architecture. The advantages of this proposed architecture is efficient in speed and area(less resources used, such as less number of multipliers and adders) and is Flexible in design Example, the same architecture can be extended for 16 -bit, 64- bit etc multiplication.

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